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MOCVD-Grown MoS₂ Wafers as a Transfer-Free Platform for Top-Gate Devices via Dry Interface Engineering

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ABSTRACT

We uncover the electronic origin of hidden interfacial doping in monolayer MoS₂ single-crystal wafers grown on sapphire by metal–organic chemical vapor deposition (MOCVD) and establish a transfer-free top-gate device platform. Despite structural perfection, as-fabricated devices exhibit degenerate electron doping and lack a clear off state. Hall measurements quantify an interfacial electron density of $2.7 \times 10^{12} \text{ cm}^{-2}$, evidencing substantial charge transfer across the nominal van der Waals interface. Interface-sensitive spectroscopy, lateral force microscopy, and thermal desorption analysis reveal a buried sulfate-derived layer accompanied by a water-like interfacial structure that acts as an intrinsic electron donor. A purely dry H₂/Ar annealing process selectively removes these species, suppressing charge transfer and restoring intrinsic FET characteristics without transfer or wet processing. Through this dry interface engineering approach, we demonstrate MOCVD-grown single-crystal MoS₂ wafers as a robust, transfer-free platform for the reliable evaluation of intrinsic gate stacks and device performance.

1 | Introduction

For the 1-nm technology node, two primary strategies have been explored to realize transition metal dichalcogenide (TMDC) nanosheet devices [1]. The first involves the epitaxial growth of single-crystalline TMDCs on sapphire substrates, followed by transfer onto Si substrates for device fabrication [2, 3]. The second relies on direct device fabrication via localized and selective low-temperature growth of TMDCs on amorphous sacrificial layers formed on Si substrates [4, 5]. Although substantial progress has been achieved, both approaches generally require multistep and complex processes, particularly at the 10-nm scale. While TMDC

nanosheet architectures are undoubtedly important for beyond-Si technologies, an equally critical challenge lies in establishing a device platform that enables rigorous and intrinsic evaluation of device performance. In this context, single-crystalline MoS₂ grown on sapphire substrates should be regarded not merely as a transferable film, but as a wafer platform itself, enabling direct device fabrication and systematic evaluation of gate-stack integration and electrical reliability, inherently free from defects and contamination introduced during transfer.

Recent advances have enabled wafer-scale growth of TMDCs on wafers up to 12 inches [6–8], marking a major milestone

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in scalable 2D synthesis. Despite this technological maturity, most TMDC films grown on sapphire by powder-source chemical vapor deposition (CVD) or metal-organic CVD (MOCVD) are still transferred onto Si substrates prior to device characterization [9–12] and integrated circuit formation [13, 14]. While limited reports exist for top-gate devices directly fabricated on powder-CVD-grown MoS₂ wafers [15–18], analogous demonstrations based on MOCVD-grown MoS₂ wafers remain absent.

The TMDC/sapphire interface directly governs top-gate device operation, yet its electronic impact remains poorly understood. Recent structural and spectroscopic studies have revealed that the TMDC/sapphire interface is not a chemically inert van der Waals interface. Cross-sectional high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) [19, 20] and X-ray standing wave excited fluorescence (XSW-XRF) [21] measurements have identified chalcogen species on the sapphire surface in MoS₂/sapphire and WSe₂/sapphire systems, accompanied by interfacial water molecules [22]. Conventionally, sapphire c-plane substrates are prepared by air annealing to form step-terrace structures prior to MOCVD growth [23]. However, atomically step-engineered sapphire surfaces can undergo chemical modification upon air exposure, potentially forming aluminum hydroxide layers [24]. Such interfacial species can profoundly influence the electronic structure and carrier transport of TMDCs.

Thus, despite the high crystallographic completeness of monolayer (1L) MoS₂ single-crystal wafers, the role of the MoS₂/sapphire interface in governing electron transport and device reliability remains unresolved. Here, we fabricate top-gate FETs directly on 1L MoS₂ single-crystal wafers grown on sapphire via a self-aligned and self-limiting process, without any transfer steps. The as-fabricated devices exhibit no well-defined off-state and a markedly shifted threshold voltage, indicative of substantial background electron doping. Interface-sensitive X-ray photoelectron spectroscopy (XPS) and atomic force microscopy (AFM) identify sulfur-related and interfacial water-like species at the bottom MoS₂/sapphire interface, implicating interfacial charge transfer as the dominant doping source. Hall measurements corroborate this interpretation, yielding an electron density of $2.7 \times 10^{12} \text{ cm}^{-2}$. Removal of the interfacial layer by a purely dry H₂/Ar treatment at 400°C restores clear off-state behavior and well-defined field-effect transistor (FET) characteristics, establishing MOCVD-grown MoS₂ wafers as a viable van der Waals semiconductor platform for top-gate devices.

2 | Results and Discussion

We have recently demonstrated the single-crystalline growth of 1L MoS₂ on a 2-inch sapphire wafer via self-aligned and self-limited MOCVD growth, employing MoO₃Cl₂ as the molybdenum precursor [25]. In this study, 1L MoS₂ films grown at 975°C and 1025°C are primarily used for FET fabrication, as these growth temperatures ensure single-crystalline film formation and high carrier mobility. When MoS₂ films grown at other temperatures are employed, the corresponding growth conditions are explicitly stated. As shown in Figure 1a,b, top-gate FETs with a 20-

nm Al₂O₃/1-nm Er₂O₃ gate dielectric [26, 27] and gate overlap structure were directly fabricated on this MoS₂ wafer without transfer to another substrate (Materials and Methods, Figure S1). Benefiting from the large-area uniformity, massive integration of various devices can be realized. As shown in Figure 1c, however, the top-gate FET cannot be switched off, exhibiting only about one order of current modulation even under very large negative gate bias (up to −17 V). This heavily electron-doped behavior indicates strong charge transfer originating from extrinsic factors (Figure 1).

Three possible origins of charge transfer are expected. First, the hole trapping by trap sites at the surface of top-gate insulator or inside can be expected due to the strong negative shift of threshold voltage (V_{th}). The second origin may be the sulfur vacancy (V_{S}) introduced by top-gate deposition, which serves as the electron donor. Since off-state cannot be observed in $I_{\text{D}}-V_{\text{TG}}$, the defect density should be much larger than 10^{13} cm^{-2} . In fact, according to the low-temperature photoluminescence (PL) measured at 4 K after top-gate deposition, as shown in Figure S2, the defect-bounded exciton at ~1.7 eV is not observable [28]. This indicates that V_{S} in MoS₂ is less than 10^{13} cm^{-2} [29, 30], which excludes sulfur vacancy for the dominant origin of the large V_{th} shift. The third origin is the charge transfer from the unclarified surface layer formed on the sapphire substrate during the MOCVD growth, as described in the Introduction. Based on this discussion, the charge transfer from the top-gate insulator and the bottom substrate should be clarified.

In order to eliminate the influence of the unclarified surface layer on the sapphire substrate, the MoS₂ film was transferred from the growth substrate onto a fresh sapphire substrate using a PMMA-assisted process, and top-gate devices were subsequently fabricated. The transfer procedure is described in Figure S3. As shown in Figure 1c, well-defined switching characteristics were clearly observed, with an on/off ratio of 10^6 , a subthreshold swing (SS) of ~270 mV/dec, and V_{th} of approximately −12 V. These results indicate that suppression of charge transfer can be achieved by appropriately decoupling the interaction between MoS₂ and the sapphire substrate. It should be noted, however, that V_{th} remains on the negative side, which is likely attributable to residual charge transfer from the pristine α -Al₂O₃ substrate and/or from the top-gate insulator.

Qualitatively, by transferring the MoS₂ film onto a fresh sapphire substrate and thereby eliminating charge transfer from the unclarified surface layer on the original sapphire substrate, the off-state could be successfully observed. Here, instead of relying on V_{th} shifts extracted from transfer characteristics, a quantitative discussion is conducted by estimating the carrier concentration through Hall measurements. Accurate determination of the Hall voltage requires that (i) the contacts at the Hall terminals be ohmic, and (ii) the width-to-length ratio (W/L) of the Hall channel be less than 1/3, such that the geometry factor can be neglected [31]. Benefiting from the wafer-scale MoS₂ film, the required Hall bar structure under the maximum magnetic field of 1 T can be readily fabricated, as shown in the inset of Figure 1d. The carrier concentration was then extracted from the magnetic-field dependence of the Hall resistance, as shown in Figure S4.

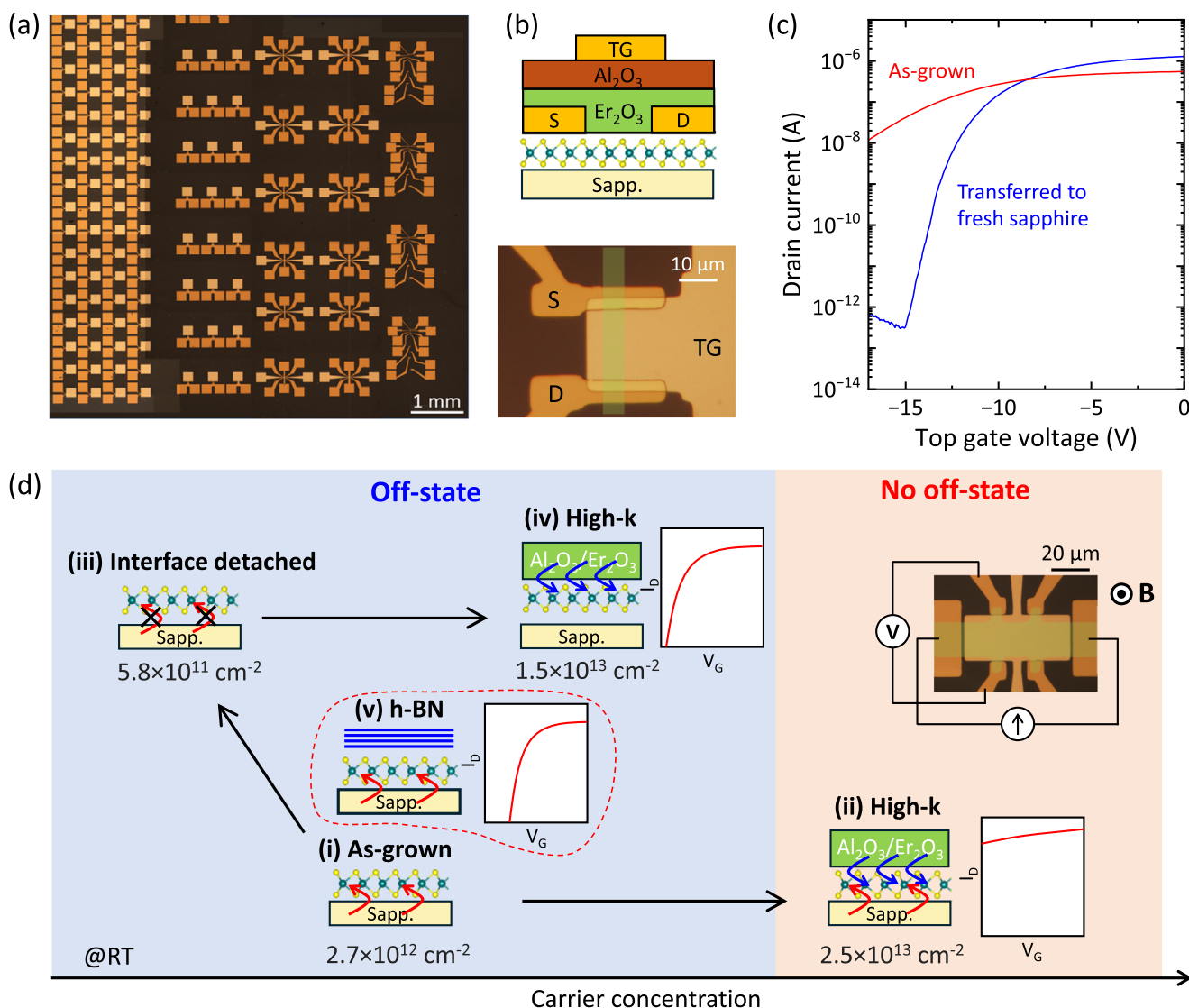


FIGURE 1 | (a) Optical image of MoS₂ devices fabricated on a sapphire substrate. (b) Schematic illustration and magnified optical image of a top-gate MoS₂ FET. hatched region is 1L MoS₂. (c) Transfer characteristics of the top-gate MoS₂ FETs. (d) Schematic illustration summarizing the overall charge-transfer picture. The electron densities at $V_G = 0$ V, determined by Hall measurements, are indicated for the different situations. The inset shows an optical image of a Hall-bar-type top-gate MoS₂ FET.

Figure 1d summarizes the carrier concentrations extracted from Hall measurements for different sample conditions under floating gate conditions. The as-grown sample (i) exhibited a carrier concentration of $2.7 \times 10^{12} \text{ cm}^{-2}$, whereas deposition of the gate dielectric (ii) led to a pronounced increase to $2.5 \times 10^{13} \text{ cm}^{-2}$, resulting in the inability of the device to reach the off-state. In contrast, the sample transferred onto a fresh sapphire substrate (iii) showed a substantial reduction in carrier concentration to $5.8 \times 10^{11} \text{ cm}^{-2}$. After deposition of the gate dielectric on this transferred sample (iv), the carrier concentration increased to $1.5 \times 10^{13} \text{ cm}^{-2}$; however, a clear off-state was still observed. By comparing these results, the amount of charge transfer from the unclarified surface layer on the sapphire substrate to MoS₂ is quantitatively estimated to be on the order of 10^{12} cm^{-2} . This value is not as large as initially anticipated. Consistently, when *h*-BN (v), which is known to induce minimal charge transfer [32], was employed as the top-gate dielectric, a well-defined off-current was clearly observed, as shown in Figure S5. These results clearly

demonstrate that substrate-induced charge transfer determines the initial carrier concentration in MoS₂, which in turn critically governs the FET operation after gate dielectric deposition.

To elucidate the origin of the charge transfer on the order of 10^{12} cm^{-2} to MoS₂ on sapphire, the MoS₂/sapphire interface was investigated in detail. Figure 2a shows an AFM height image of an as-grown MoS₂ wafer, showing continuous MoS₂ coverage over the sapphire steps across the entire surface. Magnified terrace images (Figure 2b,c) reveal uniform height modulations of approximately 0.3 nm extending over the whole area, which is comparable to the characteristic dimension of a single water molecule [33, 34]. To determine whether this water-like layer resides on the MoS₂ surface or at the MoS₂/sapphire interface, atomic-resolution lateral force microscopy (LFM) measurements [35, 36] were performed, as shown in Figure 2d. LFM visualizes atomic-scale friction and lattice anisotropy via the torsional response of the AFM cantilever and, importantly,

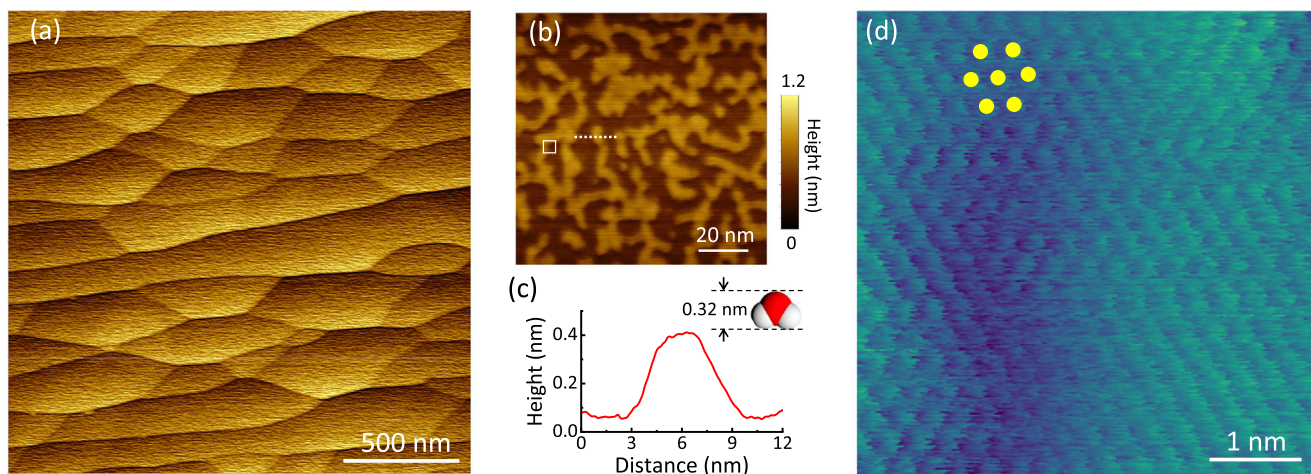


FIGURE 2 | (a) AFM topographic image of as-grown MoS₂ on sapphire substrate. (b) Magnified AFM image of the sapphire terrace region. (c) Height profile taken along the white line in (b). The inset illustrates a schematic of H₂O molecules. (d) LFM image acquired from the box region in (b). The yellow circle corresponds to the topmost S atom of the MoS₂.

enables atomic-resolution imaging even on insulating substrates such as sapphire, which is not accessible by scanning tunneling microscopy, thereby allowing direct observation of the topmost S atoms of the MoS₂ surface immediately after MOCVD growth. LFM images acquired at the boxed region in Figure 2b exhibit a continuous sulfur atomic lattice (yellow circles) across the height-modulated area, indicating that the 0.3-nm layer is buried at the MoS₂/sapphire interface rather than residing on the MoS₂ surface. Under MOCVD growth conditions near 1000°C, the sapphire surface is presumed to be Al-terminated [37] and thus hydrophobic. Given the intrinsically hydrophobic nature of MoS₂, the penetration of water molecules into the MoS₂/sapphire interface would not be expected. However, the interfacial water-like feature at the MoS₂/sapphire interface has also been reported for MoS₂ films grown by MOCVD using different Mo precursors [22] and by powder CVD [38], suggesting that this phenomenon is intrinsic to MoS₂/sapphire heteroepitaxy.

The MoS₂/sapphire interface was further investigated by XPS at different take-off angles (TOAs), as shown in Figure 3a,b. In addition to 1L MoS₂, multilayer (ML) MoS₂ (3–5 layers) was synthesized on a sapphire substrate by employing Mo(CO)₆ as an alternative molybdenum precursor and extending the growth time to 210 min. For 1L MoS₂, the S 2p doublet peaks are clearly resolved, indicating high chemical uniformity. Nevertheless, an S⁶⁺ component is observed at ~168 eV for both TOAs (10° and 90°). In contrast, no S⁶⁺ component is detected in ML MoS₂ when measured at a TOA of 25°, where the photoelectron signal from the MoS₂/sapphire interface is effectively suppressed. These results indicate that the S⁶⁺ species is localized within ~1–2 nm from the MoS₂/sapphire interface. The Mo 3d spectra of both 1L and ML MoS₂ are dominated by the Mo⁴⁺ component from MoS₂, accompanied by a very small Mo⁶⁺ contribution attributable to MoO₃. Since MoO₃ is observed even in ML MoS₂, it is likely associated with local oxidation of MoS₂ at the surface or within the limited grains.

In previous studies, both S⁶⁺ and Mo⁶⁺ components have commonly been attributed to severe oxidation of MoS₂ [39–41]. However, the present results clearly distinguish their origins:

while the Mo⁶⁺ component appears in both 1L and ML MoS₂, the S⁶⁺ component assigned to SO₄²⁻ is detected exclusively in 1L MoS₂ on sapphire and is absent in ML MoS₂. This suggests that SO₄²⁻ is a chemical species specific to the MoS₂/sapphire interface. Although the energy region around 170 eV has often been neglected in XPS studies for MoS₂ growth, recent MOCVD reports [21] have also identified weak SO₄²⁻-related S⁶⁺ signals, and XSW-XRF measurements have indicated sulfur termination on sapphire surfaces. Moreover, time-of-flight secondary ion mass spectrometry (ToF-SIMS) measurements [42, 43] (Figure 3c and Figure S6) reveal a slight decrease in interfacial sulfur with increasing MOCVD growth temperature of MoS₂, suggesting that the formation of interfacial sulfur species depends on growth conditions.

It is important to note that SO₄²⁻ species have been reported to bind to Al atoms on sapphire surfaces [44]. Moreover, the strong hygroscopic nature [44, 45] of SO₄²⁻ provides a plausible explanation for the penetration of interfacial water between MoS₂ and the sapphire substrate after the MOCVD growth, despite the intrinsic hydrophobicity of MoS₂. Contact-angle measurements in Figure S7 show that while the as-grown MoS₂ surface is hydrophobic, the sapphire surface exposed after MoS₂ delamination remains hydrophilic, which is compatible with the presence of a hydrophilic interfacial environment, even though the specific interfacial species may be altered during the delamination process. Indeed, MoS₂ grown on the sapphire substrate by powder-source CVD has been reported to exhibit electron doping on the order of 10¹³ cm⁻² due to interfacial water incorporation [38] due to the hydroxylation of the sapphire surface [46, 47]. This may also originate from the strong water-adsorbing nature of SO₄²⁻ formed at the MoS₂/sapphire substrate.

Based on the representative S⁶⁺ species suggested by XPS analysis, density functional theory (DFT) calculations in Figure S8 suggest that SO₃ adsorbed on Al-terminated sapphire surface is a plausible candidate among two energetically stable sulfur(VI)-related surface configurations, namely SO₃ and SO₄H₂. As shown in Figure 3d, the ordered interfacial water molecules on the relatively smooth interfacial morphology may account for the

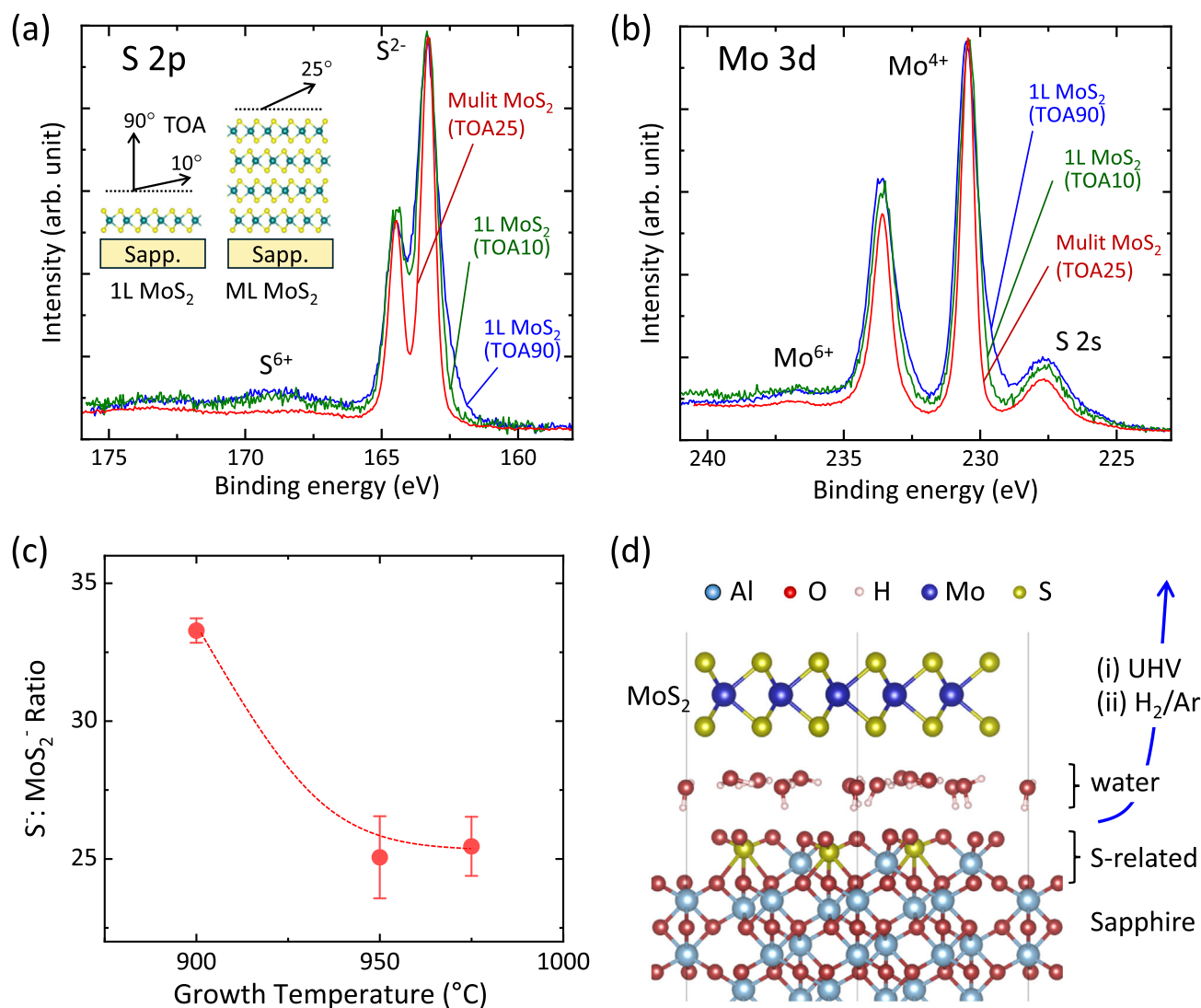


FIGURE 3 | XPS spectra of (a) S 2p and (b) Mo 3d measured at different TOAs for monolayer (1L) MoS₂ and multilayer (ML) MoS₂. (c) S²⁻:MoS₂ ratio as a function of MOCVD growth temperature obtained by ToF-SIMS. (d) Conceptual model of sulfur(VI)-related species and interfacial water layer at the MoS₂/sapphire interface suggested by DFT calculations. Detailed discussions of the DFT-derived interface structures are provided in Figure S8.

~0.3 nm modulation observed by AFM. Moreover, the calculations suggest that these polar species can coexist without inducing significant structural instability. Since the simulated structure has not yet been experimentally verified, it should be regarded only as a conceptual interfacial model intended to facilitate understanding of the presence of a sulfur(VI)-related interfacial layer together with a water-like layer. In reality, as clarified in our previous TEM studies on as-grown MoS₂/sapphire interfaces [48], the interface is not a vacuum gap but consists of an amorphous intermediate layer, and the sulfur(VI)-related species are not arranged in an ordered manner but are instead expected to form a more random structure. Detailed discussions of the two different interface structures are provided in Figure S8.

Here, instead of employing a wet transfer process using KOH to transfer MoS₂ onto a fresh substrate, we focused on a dry approach that directly cleans the MoS₂/sapphire interface. Thermal desorption mass spectrometry (TDS) was performed to identify species desorbed from a MoS₂/sapphire wafer during annealing under ultra-high vacuum (UHV) conditions of approx-

imately 4×10^{-8} Pa, using a quadrupole mass spectrometer (QMS) [49–51]. As shown in Figure 4a, pronounced H₂O desorption ($m/z = 18$) is observed, accompanied by weaker signals at $m/z = 32, 34, 48, 64$, and 96 , which may originate from S-containing species. No clear desorption of Mo-related species was detected within our detection limit. As detailed in Figure S9, the apparent TDS intensity can be artificially distorted by transient total pressure rises during high-flux desorption events. By comparing S-related channels with adjacent background references, SO ($m/z = 48$) and SO₂ ($m/z = 64$) are identified as the dominant S-containing desorption products during UHV annealing. These observations clarify the chemical species evolving from the MoS₂/sapphire interface during UHV annealing, providing a basis for understanding the subsequent changes in optical and electrical properties.

We further investigated the effects of annealing under UHV and H₂/Ar gas environments using rapid thermal annealing (RTA), as evaluated by photoluminescence (PL) measurements (Figure 4b). These PL measurements were performed during the device

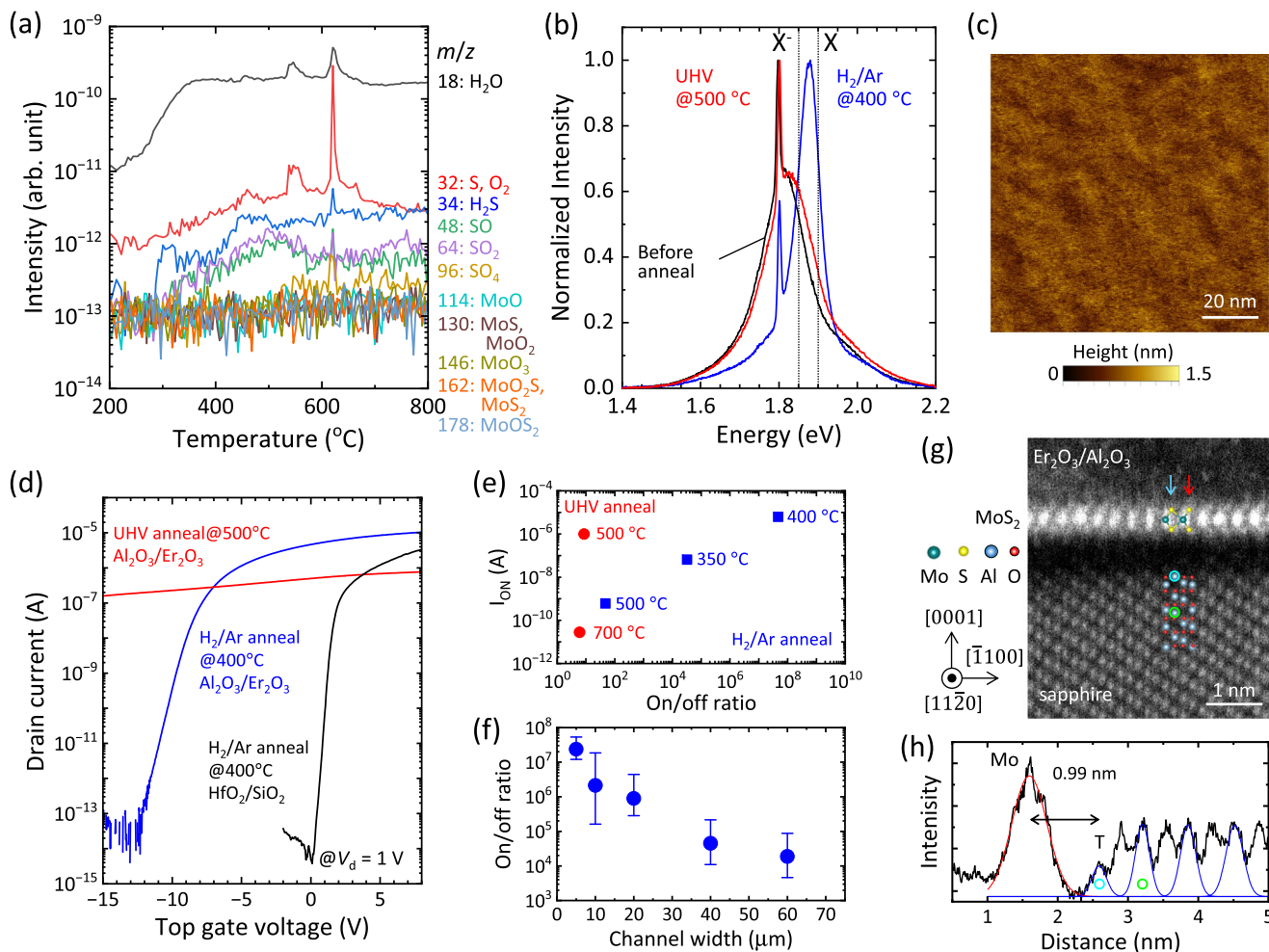


FIGURE 4 | (a) TDS spectra of as-grown MoS₂ on the sapphire substrate. (b) PL spectra of before anneal, UHV anneal and H₂/Ar anneal. X and X⁻ denote neutral exciton and negatively charged trion, respectively. (c) AFM topographic image of H₂/Ar annealed MoS₂ on sapphire substrate. (d) Transfer characteristics of the top-gate MoS₂ FETs with UHV and H₂/Ar annealing. (e) I_{ON} as a function of on/off ratio for Al₂O₃/Er₂O₃ top gate MoS₂ FETs with UHV and H₂/Ar annealing. (f) Current on/off ratio as a function of channel width for HfO₂/SiO₂ top gate MoS₂ FETs. (g) HAADF-STEM image of the MoS₂/sapphire interface in a top-gate MoS₂ FET with H₂/Ar annealing. (h) Image intensity along the [0001] direction extracted from (g). The topmost Al atom is labeled T. The Mo–Al interatomic distance was determined by Gaussian fitting of Mo (red) and Al (blue, corresponding to Al–I atomic columns) peaks. The Al positions indicated by light blue and light green circles correspond to those in the atomic structural model of (g).

fabrication process, as detailed in Figure S1. As-grown MoS₂ on sapphire substrate exhibited a clear trion emission, indicating electron doping from the substrate. After UHV annealing at 500 °C, the PL peak position exhibited only minor changes, indicating that the doping level remained largely unaffected. In contrast, annealing at 400 °C under H₂/Ar gas induced a clear transition from trion- to exciton-dominated emission [52], suggesting a reduction in electron doping. Moreover, Raman peaks remained unchanged after both UHV and H₂/Ar annealing, as shown in Figure S10. Considering the TDS results, both physically and chemically adsorbed H₂O are expected to desorb within this temperature range under both annealing conditions, indicating that water removal alone cannot explain the distinct PL response. Therefore, the difference between UHV and H₂/Ar annealing is attributed to the reduction of SO₄⁻-related interfacial structures by hydrogen, followed by their removal from the interface as volatile species such as SO₂ or H₂S, according to reactions such as (i) SO₄²⁻ + H₂ + 2H⁺ → SO₂↑ + 2H₂O↑ and/or (ii) SO₄²⁻ + 4H₂ + 2H⁺ → H₂S↑ + 4H₂O↑. Although SO- and SO₂-related signals were

detected during UHV annealing in TDS, the negligible change in PL suggests that UHV treatment alone does not sufficiently modify the interfacial sulfur-related states responsible for charge transfer. Indeed, the AFM surface morphology shown in Figure 4c confirms that the interface becomes flatter after the desorption of water-related species.

As shown in Figure S1, top-gate devices with a channel width of 10 μm and a channel length of 20 μm were fabricated by additionally applying UHV or H₂/Ar gas annealing. The I_D–V_{TG} characteristics in Figure 4d reveal that sufficient current turn-off is not achieved after UHV annealing, whereas a clear off-state is obtained after H₂/Ar gas annealing. This dry H₂/Ar annealed device exhibit better ON current than the wet transferred devices, as shown in Figure S11a. Moreover, as shown in Figure 4e, device performance degrades at elevated annealing temperatures, indicating that 400 °C under H₂/Ar provides the optimal annealing condition. It should be emphasized that detailed PL analysis reveals that the MoS₂ lattice remains largely intact up to

450°C, while degradation begins to occur at higher temperatures, as shown in Figure S12. This observation is consistent with previous reports [53, 54], where MoS₂ decomposition under H₂-containing atmospheres was observed only above ~500°C. To further improve the transfer characteristics, the buffer layer formation and subsequent high-*k* deposition were optimized using 1-nm SiO₂ interfacial layer followed by 25-nm ALD-grown HfO₂. As shown in Figure 4d and Figure S11, this optimization yields sharp switching behavior with SS = 180 mV/dec, which is attributed to the suppression of charge transfer from the buffer layer. Notably, the removal of SO₄-related interfacial structures by H₂/Ar annealing is kinetically limited, resulting in a strong dependence on channel width. As shown in Figure 4e, a pronounced improvement is observed when the channel width is reduced to 5 µm.

Finally, the MoS₂/sapphire interfacial structure in a top-gate MoS₂ FET with H₂/Ar annealing was investigated by HAADF-STEM, as shown in Figure 4g and Figure S13. The observed epitaxial relationship between MoS₂ and sapphire, where Mo atoms are located atop the Al (1100) planes and the Mo-S bond length is longer on the left side of Mo than that on the right side, together with the Al-I terminated sapphire surface structure [55] and the presence of an amorphous interfacial layer at the MoS₂/sapphire interface, are consistent with our previous TEM observations of as-grown MoS₂ on sapphire [48]. However, the intensity profile in the depth [0001] direction, measured along a *m*-plane of sapphire, shows that the Mo-T distance (T: topmost Al) was found to increase from 0.86 to 0.98 nm after the top-gate device fabrication process including the H₂/Ar annealing (Figure 4h). This increase in the Mo-T distance could be attributed to the elimination of interactions between MoS₂ and the SO₄-related interfacial layer, which is consistent with the reduced charge transfer to MoS₂ inferred from the PL and *I*_D-*V*_{TG} characteristics. Nevertheless, the origin of the relatively long Mo-T distance of 0.99 nm requires further investigation.

3 | Conclusion

In summary, we demonstrate that a dry H₂/Ar annealing process effectively restores the switching behavior of MoS₂ FETs fabricated directly on sapphire by removing the interfacial layer at the MoS₂/sapphire interface. This transfer-free, wafer-compatible dry process establishes MOCVD-grown MoS₂ on sapphire as a practical van der Waals semiconductor platform for systematic gate-stack and device studies.

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Conflicts of Interest

The author declares no conflicts of interest.

Data Availability Statement

The data that support the findings of this study are available on request from the corresponding author. The data are not publicly available due to privacy or ethical restrictions.

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Supporting Information

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